International Journal of Electrical and Electronics Research ISSN 2348-6988 (online)
Vol. 3, Issue 4, pp: (87-93), Month: October - December 2015, Available at: www.researchpublish.com

Performance Analysis of a 1-Bit Full Adder Using 180nm Technology

[1] M. HEMALATHA [2] A. NIVETHA [3] B. NANDHINI

[1] M.E AP/ECE Vivekanandha College of Engineering for Women, Tamilnadu, India

[2,3] M.E VLSI DESIGN Vivekanandha College of Engineering for Women

Abstract: **Increased usage of battery operated portable devices demands VLSI and ultra large scale integration (ULSI) designs with an improved power delay characteristics. Full adder being one of the most fundamental building block of all the circuit applications. A 1-bit full adder design employing both complementary metal oxide semiconductor (CMOS) logic and transmission gate logic is designed. The circuit was implemented for a single bit using tanner tool in 180nm technology and the parameters such as power and delay were compared with the existing designs of complementary pass transistor logic (CPL), transmission function adder (TFA), transmission gate adder (TGA), Hybrid pass logic with static CMOS output drive full adder (HPSC) and so on. For 180nm technology, the average power consumption was found to be extremely low with moderately low delay resulting from the deliberate incorporation of very weak CMOS inverters coupled with the strong transmission gates. The same design can further extend for implementing 32 bit full adder also. The present implementation was found to offer significant improvement in terms of power and speed.**

Keywords: **CMOS, TGA, CPL, HPSC, TFA.**

1. INTRODUCTION

Wireless communication plays an important role in upgrading communication technology. The increased usage of the battery operated portable devices like cellular phones, personal digital assistants (PDAs) and notebooks demands supports wireless transmission and it requires VLSI and ultra large scale integration designs with a improved power delay characteristics. Full adder being one of the most fundamental building block of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years. Different logic styles each having its own merits and demerits. The full-adder circuit adds three one-bit binary numbers (C A B) and outputs two one-bit binary numbers, a sum (S) and a carry (C1). The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers. The carry input for the full-adder circuit is from the carry output from the circuit above itself in the cascade. The carry output from the full adder is fed to another full adder below itself in the cascade. The demand and popularity of the portable electronics is driving the designers towards smaller silicon area, lesser power consumption and lesser delay. Full Adders are basic blocks of many circuits, especially in Arithmetic operations performed by processors, compressors, comparators, floating point unit and so on. There are many standard implementations in designing the Full Adder. Although the functionality is same, the way of producing the intermediate nodes and transistor count is varied. In different logic styles, one performance aspect is achieved at the cost of others. Small area and high performance are two conflicting constraints.

The power consumed for any given function in CMOS circuit must be reduced for either of the two different reasons: One of these reasons is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power dissipation is worthwhile as long as it doesn't degrade overall circuit performance. The other reason is to save energy in battery operated instruments same as electronic watches where average power is in microwatts The logic style used basically influence the size, speed, wiring complexity and power dissipation. Circuit Size depends on the number of transistors, their sizes and on the wiring complexity. In the second section various styles of Full Adder

using Majority Function and the proposed Full Adder cell is implemented. In the third section simulation results, layout of the Proposed Full Adder is provided and comparison of power consumption for different power supply voltages and Area for different implementations are provided. In conventional full adder circuits, we use CMOS technology i.e. PMOS and NMOS are used as a switch in complementary mode. Such applications of NMOS and PMOS as a switch is called pass transistor logic. In Transmission Gates, both NMOS and PMOS transistors are combined in parallel fashion. When performance of both the circuits was compared, transmission gate circuit consumed less power as compared to the pass transistor circuit designed using CMOS logic.In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Pass transistor logic often uses fewer transistors, runs faster, and requires less power than the same function implemented with the same transistors in fully complementary CMOS logic. In conventional logic families input is applied to gate terminal of transistor but in PTL it is also applied to source/drain terminal. When used as pass transistor, the device may conduct current in either direction

2. DESIGN APPROACH

The full adder circuit is represented by three blocks. Module 1 and Module 2 are the XNOR modules that generate the sum signal (SUM) and module 3 generates the output carry signal (C_{out}). Each module is designed individually such that the entire adder circuit is optimized in terms of power, delay and area. These modules are discussed below in detail.

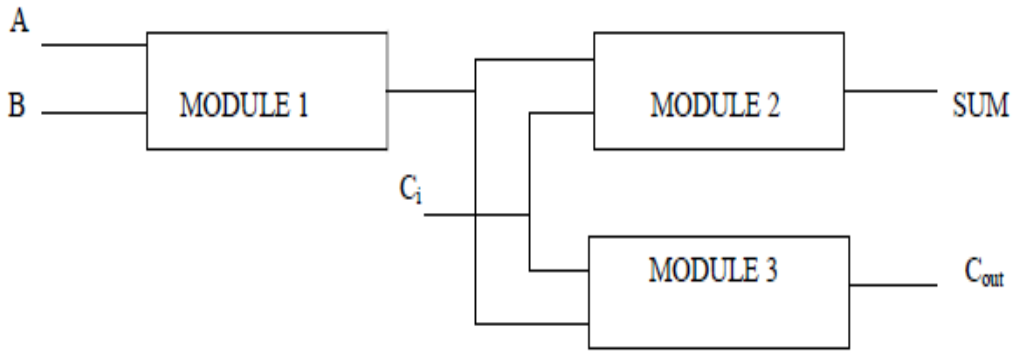


Figure 2.1 Schematic Structure of a Full Adder

2.1 MODIFIED XNOR MODULE:

In the given full adder circuit, XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility. The modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistor being small) formed by transistor Mp1 and M1. Full swing of the levels of output signals is guaranteed by level restoring transistors Mp3 and Mn3. Various XOR/ XNOR topologies have already been reported. The XOR/ XNOR reported uses four transistors but at the cost of low logic swing. To the contrary, the XOR/ XNOR used six transistors to get better logic swing compared with that of 4T XOR/ XNOR. In this paper also, the XNOR module employed 6T, but having different transistor arrangement than that of 6T XOR/ XNOR.

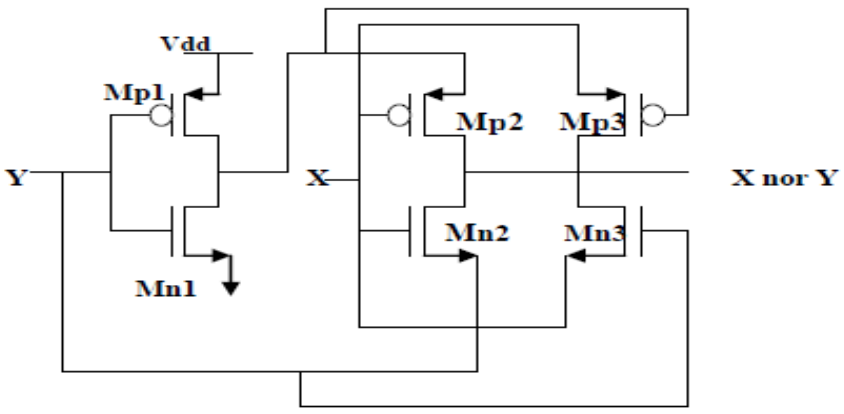


Figure 2.2 XNOR Module.

2.2 CARRY GENERATION MODULE:

In the circuit, the output carry signal is implemented by the transistors Mp7, Mp8, Mn7 and Mn8 are shown. The input carry signal (Cin) propagates only through a single transmission gate (Mn7 and Mp7) reducing the overall carry propagation path significantly. The deliberate use of strong transmission gates (channel width of transistors Mn7, Mp7, Mn8 and Mp8 is made large) guaranteed further reduction in propagation delay of the carry signal.

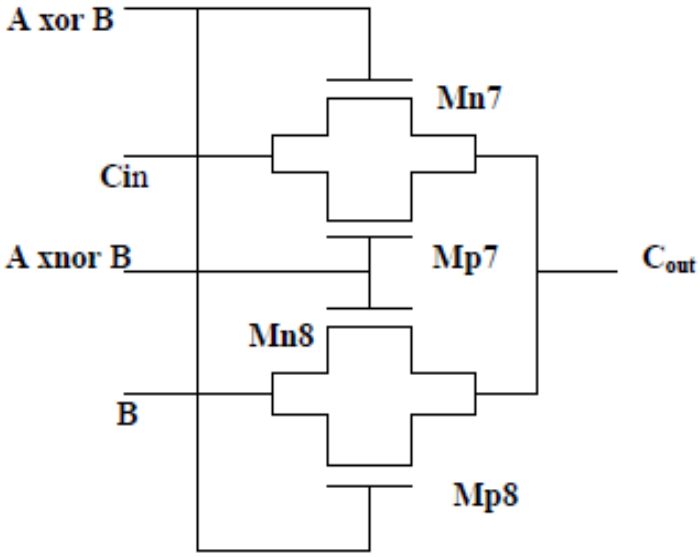


Figure 2.3 Carry Generation Module

3. OPERATION OF FULL ADDER

The detail diagram of the proposed full adder is given below. The sum output of the full adder is implemented by XNOR modules. The inverter comprised of transistors Mp1 and Mn1 generate B which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this controlled inverter is basically the XNOR of A and B. But it has some voltage degradation problem which has been removed usig two pass transistors Mp3 and Mn3. PMOS transistors (Mp4, Mp5 and Mp6) and nMOS transistors (Mn4, Mn5 and Mn6) realize the second stage XNOR module to implement the complete SUM fucntion. The condition for Cout generation has been deducted as follows:

If A=B then C_{out} = B; else C_{out}= C_{in}

The simulation of the full adder was carried out using 180nm technology and compared with the other potential adder designs reported [1]-[11] with special emphasis on design approach. The aim to optimize both power and delay of the circuit, the power-delay product (PDP) that is the energy consumption has been minimized in the proposed case. The power consumption could be minimized by mainly sizing the transistors in inverters circuits; while the carry propagation delay could be improved by mainly sizing the transistors of the transmission gates present between the paths from Cin to Cout. The given hybrid adder requires only 16 transistors whereas the other hybrid adders require more than 20 transistors. The average power consumed by the proposed full adder is significantly lower than that of other hybrid full adders. The use of less number of transistors in this paper also improved the speed. Because of reduction in average power consumption and propagation delay, the PDP of the proposed hybrid full adder is significantly improved in comparison with the earlier hybrid adders.

A single bit adder cell designed for optimum performance may not perform well under deployment to real time conditions. This is because when connected in cascaded form, the driver adder cell may not provide proper input signal level to the driven cells. The cumulative degradation may lead to faulty output and the circuit may malfunction under low supply voltages. To analyze the success of the proposed full adder during its actual use in VLSI applications, provide a realistic environment, buffers are added at the input and the output of the test bench [13], [15]. The inputs to the adder cell, are fed through the buffers to incorporate the effect of input capacitance and the outputs are also loaded with buffers to ensure proper loading condition. The proposed full adder is simulated using several test bench setup

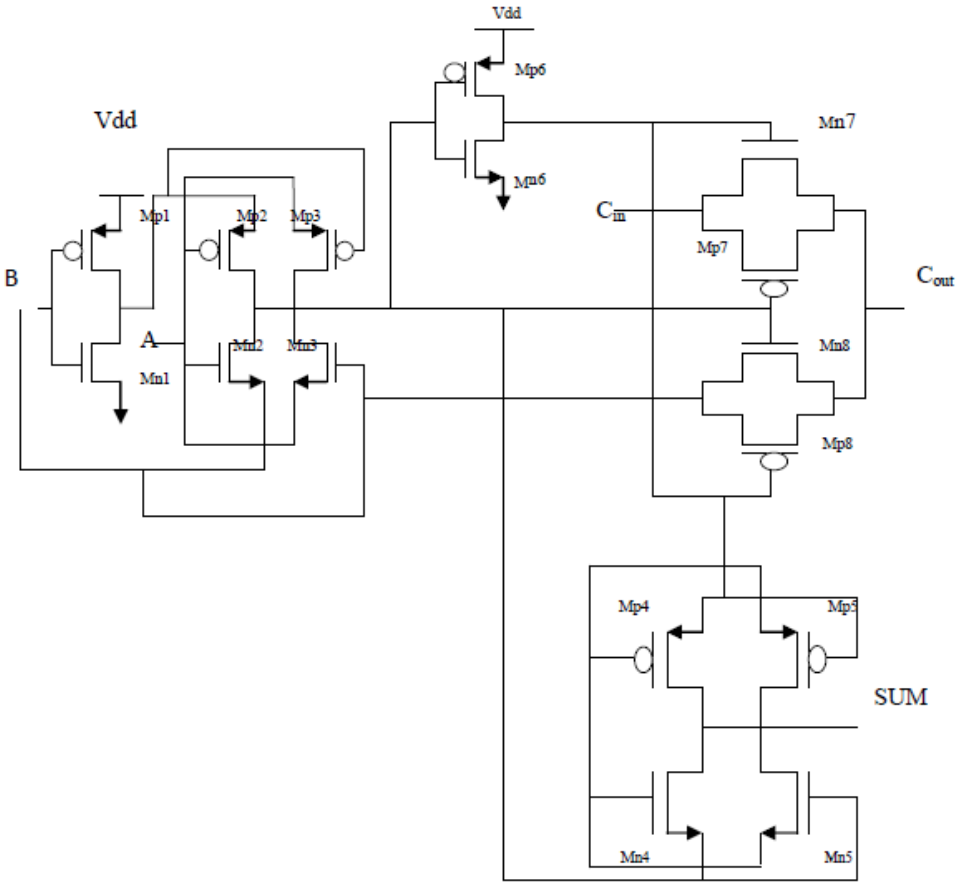


Figure 3.1 Circuit Diagram of Full Adder Using CMOS Inverter and Pass Transistor

These test benches are having the common prototype of three buffers at the input and two buffers at the output. They only differed in the number of stages of adder cells used in between the input and output of the simulation setup. The number of stages varied starting from two and increased gradually. It was observed that the carry propagation delay from the input to the output started rising significantly in the order of two after the third stage. Therefore, the three-stage simulation test bench is selected for simulation purpose. Further, the behavior of performance parameters (power and delay) could be measured from the second adder cell by using this test bench.

3.1 Calculation Of Power Consumption:

Power consumption of the hybrid full adder can be broadly classified into two categories: 1) static power and 2) dynamic and short-circuit power [13]–[15]. Static power, originated from biasing and leakage currents, in most of the CMOS-based implementations is fairly low when compared with its dynamic counterpart [3]. In this paper, with an aim to minimize the static power further, the weak inverters having large channel width of 800/240 nm (in 180-nm technology) for Mp1 and Mp6, respectively, and 400/120 nm (180nm technology) for Mn1 and Mn6 respectively was incorporated deliberately. The overall static power in 180-nm technology was found to be 2.139 nW which is very low when compared with the overall dynamic power (4.1563 μW). This increase in static power is possibly due to the increase in the subthreshold conduction current and gate leakage [3]. The dominant component of the power consumption, the dynamic power, arises because of charging and discharging of the load capacitances. The load capacitance, *C*load, can be expressed as a combination of a fixed capacitance, *C*fix, and a variable capacitance, *C*var , as follows:

$$Cload = Cfix + Cvar \ . \ (1) \qquad (1)$$

In this expression, *C*fix is the technology-dependent (principally originated from diffusion capacitance) and interconnect dependent capacitances. The interconnect dependent capacitance is minimized by efficient layout design in this case. On the other hand, *C*var is composed of the input capacitances of subsequent stages and a part of the diffusion capacitance at the gate output and can therefore be taken care of by proper sizing of the transistors.

$$\text{Power} = \text{VDD} * \text{fc} * \sum_{j=1}^{N} aj * Cloadj * \Delta Vj \qquad (2)$$

3.2 Calculation of Propagation Delay:

The speed of response of an adder is mainly dependent on the propagation delay of the carry signal which is usually minimized by reducing path length of the carry signal. In the present design, the carry signal is generated by controlled transmission of the input carry signal and either of the input signals A or B (when *A* = *B*). As the carry signal propagates only through the single transmission gate, the carry propagation path is minimized leading to a substantial reduction in propagation delay. The delay incurred in the propagation is further reduced by efficient transistor sizing and deliberate incorporation of strong transmission gates. Similar observations were also reported in case of other transmission gate-based approaches.

Assuming the voltage source, *V*in, to be a step waveform (for simplicity), the delay τpd*(m)* of the cascaded proposed full adders, can be evaluated by simplifying it into a first order circuit having a time constant, τ , and applying the Elmore delay approximation [3] as follows:

$$\tau\text{pd (m)} = 0.69\ [\text{R}(\text{C1} + \text{C2})\left(\frac{\text{m(m+1)}}{2}\right) + \text{mR}(\text{CL} - \text{C1})] \qquad (3)$$

The propagation delay of the proposed adder increases rapidly with the increase in the length of the adder chain (increases as the square of *m*). The simulation results incorporating the gradual increase in the number of stages of full adders also validated this second order rise in delay with increase in the number of stages. The simulation results [given figure 3.2(a)were measured for no load capacitance and the worst case carry propagation delay is represented here. Incorporation of the load capacitance increased the delay but the nature of the graph remained the same. Considering intermediate buffer delay, the total carry propagation delay for *m* stages after the incorporation of intermediate buffers can be represented as

$$\tau pd\ (m)total = \tau pd(m) + \tau pdbuf$$
$$= 0.69 + \left[R(C1 + C2)\left(\frac{m(m+1)}{2}\right) + mR\ (Cinbuf - C1)\right] + \tau pdbuf \qquad (4)$$

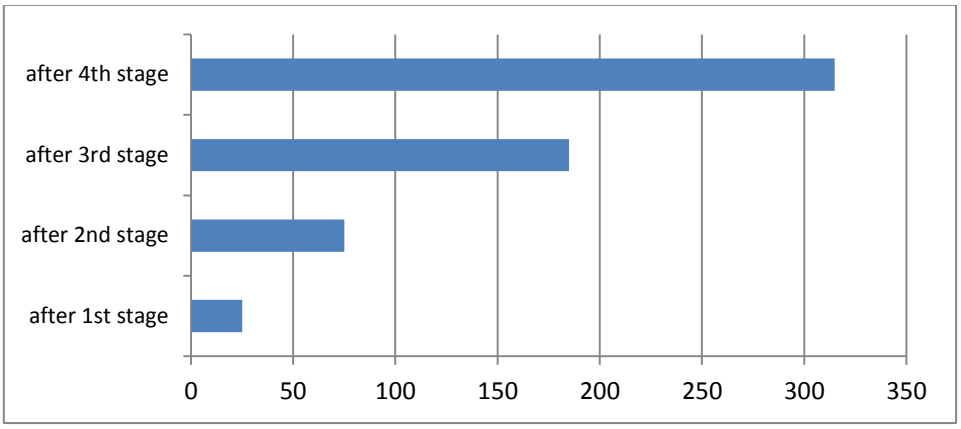
The load capacitance, *CL* , of the adder chain is given in (3) is equal to the input capacitance, *C*inbuf , of the intermediate buffer and have been replaced to derive (4). The delay of the buffers, *t*pdbuf , is independent of the number of stages, *m*, and its value is obtained by intermediate delay calculation which is found to be 326.26 ps.

R_1 = 4.2365 KΩ, C_1 = 13.792 fF and C_2 = 6.689 fF

To find the optimized number of stages, the average delay per stage ($\tau pd(m)total/m$), the value was minimized. Differentiating this average delay value with respect to m, the expression for the minimum value of m is obtained as follows:

$$m = \sqrt{((2 * \tau pdbuf)/0.69 * R * (C1 + C2)} \qquad (5)$$

From Fig. 3.2(b) and the mathematical result obtained from (5), it can be envisaged that the most optimized performance, when speed is of prime concern, is achieved using one buffer after every three stages.



Worst Case Carry Propagation Delay

Figure 3.2 (a) Total Carry Propagation Delay for Different Stages (Without Load Capacitance)

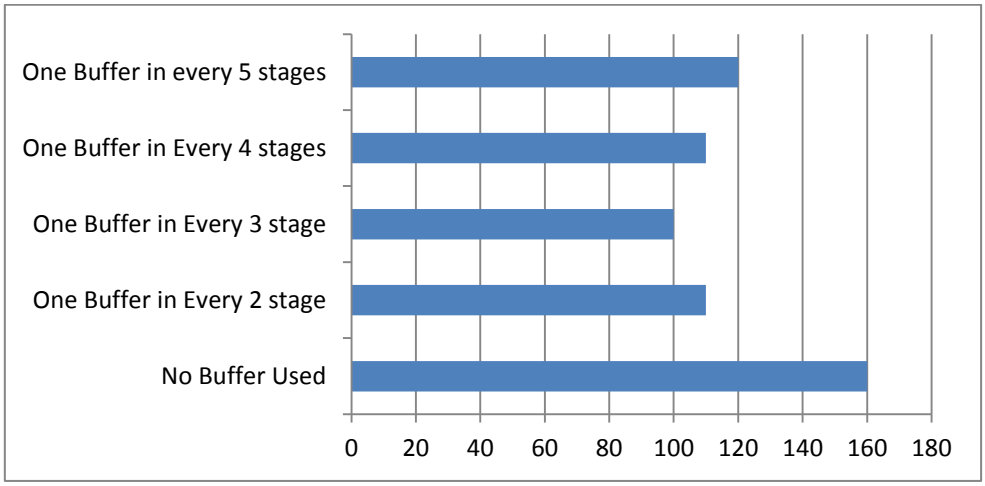


Figure 3.2 (b) Variation of Average delay with introduction of buffers at different stages

3.3 Calculation of Area of Single Bit Full Adder:

Figure 3.3 shows the layout of the proposed full adder (excluding buffers) in 180nm technology, respectively. The area in 180nm technology is 102.94μm^2. The number of transistors for the proposed hybrid full adder including buffer is 36. Hence the area of the layout of the proposed adder includig buffer in 180nm technology is 218.02 μm^2. When compared with the best design in terms of area (10 T) [14], the proposed design of the adder (excluding buffer) consumed 44.5% more area. But, the main concern of the proposed adder design was minimization of PDP, which proved to be significantly improved (~51%) with respect to 10 T design [14].

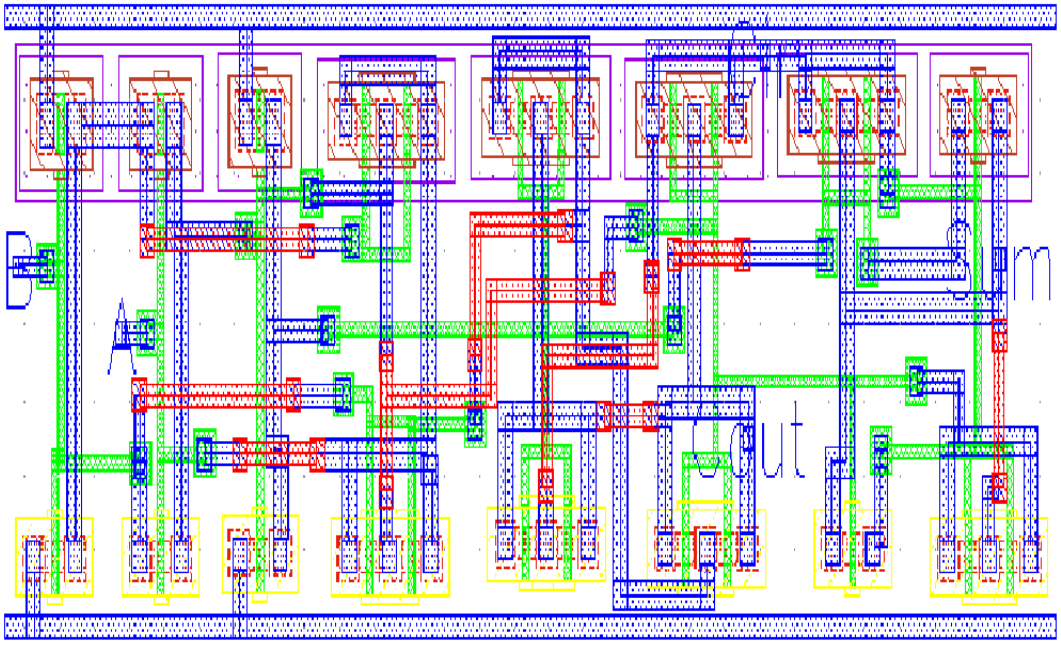


Figure 3.3 layout of the 1-bit full adder in 180nm technology

4. RESULT

The suggested method was developed and tested by using Tanner Tool with 180nm technology and compared with other standared design approaches like CMOS, CPL, TFA, TGA and other designs on a PC with an intel core i3 processor at 2.8 GHz and 4GB RAM. The proposed adder offered improved PDP compared with the earlier reports. With excluding buffer , strong transmission gates driven by weak inverters lead to fast switching speeds (224ps), for a layout area of 102.94 μm^2.

REFERENCES

[1] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, "A low-power high-speed hybrid CMOS full adder for embedded system," in Proc. IEEE Conf. Design Diagnostics Electron. Circuits Syst., vol. 13. Apr. 2007, pp. 1–4.

[2] S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energyefficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.

[3] N. H. E. Weste, D. Harris, and A. Banerjee, CMOS VLSI Design: A Circuits and Systems Perspective, 3rd ed. Delhi, India: Pearson Education, 2006.

[4] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd ed. Delhi, India: Pearson Education, 2003.

[5] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEE Proc.-Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.

[6] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[7] C. H. Chang, J. M. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.

[8] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, pp. 20–29, Feb. 2002.

[9] M. L. Aranda, R. Báez, and O. G. Diaz, "Hybrid adders for high-speed arithmetic circuits: A comparison," in Proc. 7th IEEE Int. Conf. Elect. Eng. Comput. Sci. Autom. Control (CCE), Tuxtla Gutierrez, NM, USA, Sep. 2010, pp. 546–549.

[10] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Taipei, Taiwan, Oct. 1999, pp. 713–722.

[11] M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in Proc. Int. Symp. Circuits Syst., May 2003, pp. 317–320.

[12] P. Prashanth and P. Swamy, "Architecture of adders based on speed, area and power dissipation," in Proc. World Congr. Inf. Commun. Technol. (WICT), Dec. 2011, pp. 240–244.

[13] M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, and A. Golmakani, "Design of new full adder cell using hybrid-CMOS logic style," in Proc. 18th IEEE Int. Conf. Electron., Circuits Syst. (ICECS), Dec. 2011, pp. 451–454.

[14] I. Hassoune, D. Flandre, I. O'Connor, and J. Legat, "ULPFA: A new efficient design of a power-aware full adder," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 8, pp. 2066–2074, Aug. 2010.

[15] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low-power full-adder cell for low voltage," VLSI J. Integr., vol. 42, no. 4, pp. 457–467, Sep. 2009.